## REMARKS

The Examiner has stated that claims 15-20 would be allowable. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner objected to claim 12 stating: " Claim 12 is objected to because of the following informalities: the dependency of claim 12 is unknown." In response Applicants have amended claim 12 to include its dependency on claim 7.

The Examiner rejected claims 1-3, 6-10, 12-13 under 35 U.S.C. §102(e) as being unpatentable over Tews et al. (U.S. 6,599,798) previously applied.

The Examiner rejected claims 1-14 under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. 6,373,086 previously cited, in view of level of skill of an ordinary person in the art.

The Examiner rejected claims 4-5, 11 and 14-20 under 35 U.S.C 103(a) as being unpatentable over Tews et al. as applied to claims 1-3, 6-10, 12-13 above, and further in view of Mandelman et al, both previously cited.

Applicants respectfully traverse the §102(e) and §103 (a) rejections with the following arguments.

35 USC § 102

As to claim 1, 4 and 7 the Examiner states that "Tews discloses a method of forming a buried dielectric collar around a trench, comprising: forming a trench in a substrate, fig. 2+, col. 3, lines 60+, forming a multilayer coating 20/21/24 on sidewalls and a bottom of the trench, removing a continuous band of multilayer coating from the sidewalls a fixed distance from a top of said trench to expose a continuous band of substrate in the sidewalls of said trench, etching, in the exposed trench extending into the trench, filling the lateral trench with a dielectric material to band of substrate, a lateral substrate in the sidewalls of form a buried dielectric collar, buried dielectric collar extends continuously around the trench (recess formed around the trench) , col. 4, lines 31+ and fig. 5, buried dielectric collar extends into said trench."

Applicants contend that claims 1, 4 and 7, as amended, are not anticipated by Tews et al. because Tews et al. does not teach each and every feature of claims 1, 4 and 7. In a first example, Tews et al. does not teach "forming a multilayer coating on sidewalls and a bottom wall of said trench." Applicants respectfully point out that in FIGs 2 and 3 and col. 3 line 60 to col. 4 line 19 which states:

"The process flow or integration scheme for providing a buried LOCOS collar in trench DRAMs in the present invention may be best understood by reference to *FIG. 2 which shows the DRAMs structure at a stage after a DT etch, deposition of a thin nitride layer 20,* for example, by a LPCVD (Low Pressure Chemical vapor Deposition) at about 40A thick. The DT etch is affected through a pad nitride 10, and *after deposition of the thin nitride layer 20, trench fill is accomplished with sacrificial polysilicon 22.* Thereafter, planarization and poly recess is affected to obtain a depth above the STI (Shallow Trench Isolation) level 23 at about 500 nm.

*After preparing the structure shown in FIG. 2, the structure of FIG. 3 is formed by deposition of a thin dielectric layer 21* different from the first nitride layer 20. An example of the different layer is a thin oxide layer. This layer is created, i.e., by radical assisted oxidation of the top part of the nitride layer, or by deposition of an oxide layer. The optimal thickness of this layer would range between 30 to about 50A, although other values are possible. This layer serves as a mask layer for later processing.

*Following deposition of the thin dielectric layer different from the first nitride layer, deposition of the second thin nitride layer 24 is made*, and this deposition may be by LPCVD, of a thickness from about 30 to about 50A. The purpose of this nitride layer is to protect the oxide mask layer during the sacrificial poly strip. However, the second nitride layer is optional, and this step may be skipped if the sac poly strip does not require nitride layer."

Applicants contend that if only a single layer (layer 20) coating is formed on the bottom wall of the trench and that a multi-layer (layers 20, 21 and 24) are formed on the sidewalls of the trench. However, a multi-layer (layers 21 and 24) coating is formed on a top surface of polysilicon 22 which is partially filling the trench. That the top surface of the polysilicon can not be interpreted as the bottom wall of the trench because Tews et al. makes it very clear that the polysilicon is placed in the trench *after layer 20 but before layers 21 and 24*. The Examiner is directed to the text highlighted in the quote of Tews et al. *supra*. Applicants respectfully request the Examiner explicitly state what he interprets in Tews et al. as the "a bottom wall of said trench." if the Examiner rejects Applicants argument.

In a second example, Tews et al does not teach "continuous bands comprising three or more layers of said multilayer coating remaining above and below said lateral trench after said etching." Applicants point out that in Tews et al. FIG. 4, there was never more than one layer

below where the lateral trench of FIG. 5 has been etched and in FIG. 5 there is only one layer of the multilayer coating remaining above and only one layer below the lateral trench.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 4 and 7 is not unpatentable over Tews et al. and are in condition for allowance. Since claims 2 and 3 depend from claim 1, claims 5 and 6 depend from claim 4 and claims 8-14 depend from claim 7, Applicants respectfully maintain that claims 2 and 3, 5 and 6 and 8-14 are likewise in condition for allowance.

35 USC § 103 Rejections

As to claims 1, 4 and 7 the Examiner states that "The reference(s) teach the features Mandelman et al. discloses a method of forming a buried dielectric collar around a trench, comprising: forming a trench 42 in a substrate (note, the trench bottom is not shown), fig.14C, col. 7, lines 21+, forming a multilayer coating 44/52/56 on sidewalls and a bottom of the trench, removing a continuous band of multilayer coating from the sidewalls a fixed distance from a top of said trench to expose a continuous band of substrate in the sidewalls of said trench, etching, in the exposed trench extending into the trench, fig. 14e or fig.15d, filling the lateral trench 30 with a dielectric material to band of substrate, a lateral substrate in the sidewalls of form a buried dielectric collar, fig. 15F, buried dielectric collar extends continuously around the trench (recess formed around the trench) , buried dielectric collar extends into said trench, a multiplayer coating of oxide/nitride and polysilicon layer, filling the trench with polysilicon layer 70, using resist layer in the trench and forming a oxide/nitride/polysilicon multiplayer on the sidewall of the trench, col. 7, lines 30+ and figs. 14c. since, Mandelman et al. teaches at fig. 9a_10 and col. 6, lines 6+, forming layer 52 on the sidewall and bottom wall of trench 40, then RIE etching to obtain spacer 56 on the sidewall and at col. 7, lines 28+, forming spacer layer 44/56 by using deposition and RIE, hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that mutilayer 44/52/56 formed in the trench 42 of figure 14d is formed on the sidewall and bottom wall of the trench 42 to obtain the same spacer 56 on the sidewall of the trench 42 as shown in fig. 14C."

Applicants contend that claim claims 1, 4 and 7, as amended are not obvious in view of Mandelman et al. because Mandelman et al. does not teach or suggest every feature of claims 1, 4 and 7. For example Mandelman et al. does not teach or suggest "continuous bands comprising

three or more layers of said multilayer coating remaining above and below said lateral trench after said etching." Applicants point out that in Mandelman et al. FIGs. 14d, there is only one layer (layer 52) remaining above trench 30 after etching trench 30. Layer 56 which was present in FIG. 14c not present in FIG. 14d because layer 56 is polysilicon and is removed during the silicon etch forming trench 30.

The Examiner has rejected Claims 4-5, 1 1 and 14-20 are rejected under 35 U.S.C 103 as being unpatentable over Tews et al. as applied to claims 1-3, 6-10, 12-13 above, and further in view of Mandelman et al. 6,373,086, both are previously cited. stating" The difference between the references applied above and the instant claims) is: Tews et al. teaches forming a collar in the trench with an oxide/nitride multiplayer coating but does not teaches using a resist layer and oxide/nitride and a polysilicon layer as a multiplayer coating. However, Mandelman et al. teaches at col. 7, lines 21+ and figs. 14c that using resist layer in the trench and forming a oxide/nitride/polysilicon multiplayer on the sidewall of the trench. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with a resist layer formed in the trench and using a multiplayer coating as taught by Mandelman et al. because resist layer and multiplayer coating is used as a mask for lateral etching the sidewall of the trench."

Applicants are confused by this rejection since (1) only claim 4 references resist and (2) the Examiner has allowed claims 15-20. Applicants will proceed assuming the Examiner only intended to reject claim 4 on this basis.

As to claims 4, Applicants are again confused because the Examiner states that Mandelman et al, teaches "using resist layer in the trench", but Applicants can find no reference to "using resist layer in the trench " in Mandelman et al. Applicants are further confused because

the Examiner states the rejection is based on Tews et al. in view of Mandelman et al. but gives his reason for combining references as "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with a resist layer formed in the trench and using a multiplayer coating as taught by Mandelman et al. because resist layer and multiplayer coating is used as a mask for lateral etching the sidewall of the trench."

Applicants believe this 103(s) rejection is because the reason to combine references must exist in the prior art and not in the Applicants disclosure per *In re Vaeck*, 947 F.2d 488, 493, 20 U.Sp.Q.2d 1438, 1442 (Fed. Cir. 1991).

The Examiner has cited "a resist layer in the trench" as an obvious modification of Tews etal. in view of Mandelman et al. Applicant contend that the use of two resist layers as disclosed by Applicants and defined in claim 4 as " defining a top edge of said band with a first recessed resist process; and defining a bottom edge of said band with a second recessed resist process" has not been shown by the Examiner to be obvious to one ordinary skill in the art.

Based on the preceding arguments, Applicants respectfully maintain that claim 4 is not unpatentable over Tews et al. in view of Mandelman et al. and is in condition for allowance. Since claims 5 and 6 depend from claim 4, Applicants respectfully maintain that claims 5 and 6 are likewise in condition for allowance.

**CONCLUSION**

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-458.

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